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# Analog Radio Frequency Circuits Design Technologies in Nanoscale Integrated Circuits

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***Abstract***

*The evolution of the nanoscale complementary metal oxide semi-conductors led to many issues in analog design. Gate-leakage mismatches exceeded tolerances which require active and alternative techniques of cancellation and architectures giving rise to the low voltage techniques. Hence, functionalities are been shifted to the digital domains which also include parts of both analog and digital radio frequency circuits and imperfections in them.*

***Keywords:*** *Digital control, radio frequency circuits, analog circuits, design issues*

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## INTRODUCTION

The electronic frameworks have flown up wherever in our general public. They are exceptionally shoddy in connection to their (additional) usefulness and now and then even simply get to be form things, similar to cell phones and MP3 players. Large scale manufacturing utilizing incorporated circuits is the way to minimal effort frameworks. On account of mix, board configuration gets to be distinctly simpler and with the correct programming, frameworks can be created requiring little to no effort. Today frameworks are very digitized, empowering this reconciliation in CMOS innovation.

The development in CMOS innovation is propelled by diminishing cost per-execution for advanced hardware; its pace is controlled by Moore's law. To guarantee adequate lifetime for advanced hardware and to keep control utilization at a satisfactory level, the measurement therapist is joined by bringing down of ostensible supply voltages. While this development in CMOS innovation is by definition extremely gainful for advanced circuits, this is not so for simple circuits [1–3].

Contemporary IC's are blended flag frameworks comprising of an expansive advanced center including among others a CPU or DSP and memory, frequently encompassed by a few simple interface pieces, for example, I/O, D/An and A/D converters, RF front finishes and the sky is the limit from there. From an incorporation perspective every one of these capacities would preferably be coordinated on a solitary bite the dust. For this situation the simple gadgets must be acknowledged on an indistinguishable kick the bucket from the advanced center and therefore should adapt to the CMOS development managed by the computerized circuit.

Keeping in mind the end goal to examine the need from a circuit perspective we first take a gander at the patterns in frameworks and afterward at the patterns in CMOS innovation. It's the undertaking of the circuit architect to connect the broadening simple crevice between the framework requests and the accessible CMOS innovation.

## SYSTEMS

The pattern in framework configuration is twofold. On one hand there is a pattern to

 

coordinate more usefulness in a solitary multi-reason gadget; cases of this incorporate PC's, palmtop PCs or cell phones. These frameworks comprise of a universally useful advanced estimation center, with a reconfigurable UI and with a restricted measure of devoted I/O usefulness. Utilizing these frameworks, a large number of various assignments can be completed. These assignments go from the exposed usefulness (e.g. making a telephone call) to playing music, diversions, films, and so on. Usefulness can without much of a stretch be included by including programming. In this five star of frameworks, programming is run and flags are handled in the advanced space. The computerized center of these frameworks is in this manner ideally fabricated in cutting edge CMOS innovation to get ease per calculation and in the meantime low power per calculation.

Then again there is the pattern to make more conveyed, undetectable electronic frameworks that objective at gathering or conveying information. When all is said in done, these (for the client) imperceptible frameworks are utilized to control different frameworks and in that capacity are exceptionally upgraded for one particular undertaking, for example, detecting the oil weight in an auto or RFID. These frameworks can be viewed as sensors or I/O gadgets for a bigger framework. The center of this bigger framework typically is a programmable multi-reason gadget: an arrangement of the principal kind. The tactile gadgets contain devoted sensors and correspondence equipment and little knowledge; they can be created in an innovation which is upgraded for these capacities which commonly is not progressed CMOS due to cost reasons and the little requirement for a major computerized center.

**Analog in Systems**

All frameworks need to interface with the genuine simple world. Since the flag handling primarily is done in the computerized space for productivity reasons, the required AD converters and DA converters are moving to the edge of the framework. In the meantime, generally computerized pieces, for example, I/O are turning out to be increasingly simple because of either rapid necessities or to high-voltage prerequisites. Much the same as for any simple circuit, AD converter execution comes at the cost of region and power utilization. Thus it stays gainful to put simple preprocessing circuits like intensifiers, channels and recurrence interpretation circuits in front to the ADC to unwind its execution requests.

Since the 70s specialists attempt to incorporate these circuits in CMOS innovation, which is fundamentally created for computerized circuits. The upside of coordinating simple with advanced circuits is the subsequent conservative and minimal effort single chip arrangement. Amid the eighties simple video baseband circuits were coordinated in CMOS, covering the low MHZ recurrence go. In the nineties likewise RF circuits for the low GHz range could be outlined in CMOS in light of the fact that the speed of the innovation got to be distinctly adequate in the interim. While organizations were hesitant to put RF circuits in CMOS, colleges proceeded with research and grew new methods. Today completely coordinated RF handsets, including advanced baseband and MAC layers can be created on one single CMOS kick the bucket [4–6].

Perhaps single chip CMOS handsets are not the best performing or most financially savvy arrangements today, however because of a great deal of research exertion, the issues are unraveled a tiny bit at a time.

## Analog Challenge from a System Point of View

The following test for the simple creators shape a framework perspective can be part into two bearings. The first is to utilize the innovation advances, and move to higher frequencies, similar to 60 GHz interchanges and radar. The second direction is to digitize the RF sections to achieve both higher programmability and higher flexibility for multiple standards RF. This trend is towards e.g. software radio[7,8].

## TECHNOLOGY ISSUES

In the previous couple of many years of innovation development, planar mass CMOS was scaled to lower and lower measurements, breaking predicted points of confinement to scaling constantly. In any case, there is an agreement that scaling of planar mass CMOS will stop sooner rather than later, around the 45 nm hub. In this part of the paper first some issues concerning more or less conventional CMOS scaled down to the 45 nm node; are addressed. Later, a number of items related to the successor of the planar bulk device are reviewed.

## Output Conductance Effects

One of the significant issues in simple plan is transistor pick up, and its linearity viewpoints. As appeared by Annema et al., these are enhancing with more up to date CMOS advancements gave the voltage headroom and the transistor length are not scaled down [3]. This is outlined in Figure 1: the pickup and the IP3 don't change essentially with more current advancements at steady transistor length L and at consistent voltage headroom. With lower voltage headroom the execution of transistors abatements.

In ultra-profound sub-micron (UDSM) CMOS innovations, the transistor pick up is lower constrained by prerequisites of the advanced hardware. For its strength no less than a voltage pick up of around 10 is required utilizing the base length gadgets which additionally brings about the generally frail connection between yield conductance and innovation appeared in Figure 1. In any case, scaling routine planar mass gadgets will stop on account of the issues connected with getting adequate (advanced) pick up beneath the 45 nm innovation hub. An examination of the predicted arrangements is displayed later in this paper.

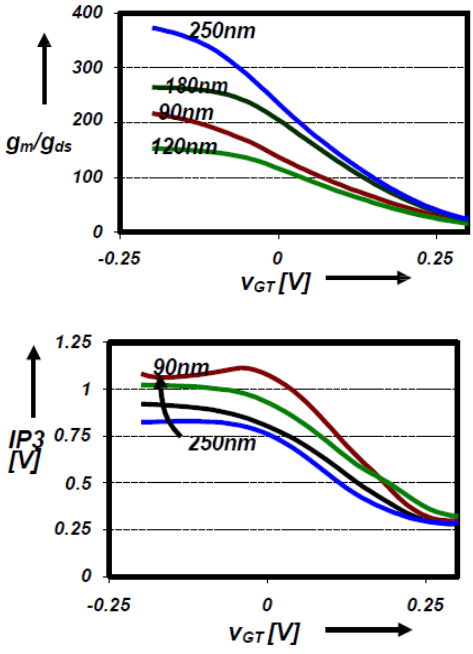

***Fig. 1:*** *Various DC-Properties of Transistors as a Function of the Gate-Overdrive Voltage with VDS =0.3 V and L=1 um for Four Technologies:* ***(a)*** *the Gain, and* ***(b)*** *the Output IP3.*

**Gate Leakage Effects**

One of the generally new impacts in ultra-profound submicron CMOS is the critical entryway spillage. One of the first areas where this became eminent was in low-frequency applications such as PLL-loopfilters and hold-circuits with long time constants. Nowadays UDSM CMOS gate-leakage may be a serious problem for analog circuit design because:

a. It poses a lower limits to the usable frequency range for integrator circuits; e.g. for filters and hold-circuits.
b. It introduces a strong relation between DC current gain and transistor length, which effectively limits accuracy.
c. Its mismatch introduces a new limit to achievable accuracy.
d. Shot noise is due to gate-current.

All these effects can easily be estimated using the $f_{gate}$ of a MOS transistor. This area-independent and fairly vDS independent parameter is for conventional MOS transistors[3].

However the maximum hold time decreases rapidly with newer technologies, down to a typical value in the low nano-second range for standard 65 nm technologies. To get an acceptable hold-time in 65 nm CMOS, either thick oxide transistors or inter-metal capacitances must be used; similar conclusions hold for PLL loop filters.

Defective entryways result in DC-input current, which sets a lower bound on the present pick up of a MOS transistor; as a harsh estimation this DC pick up is:

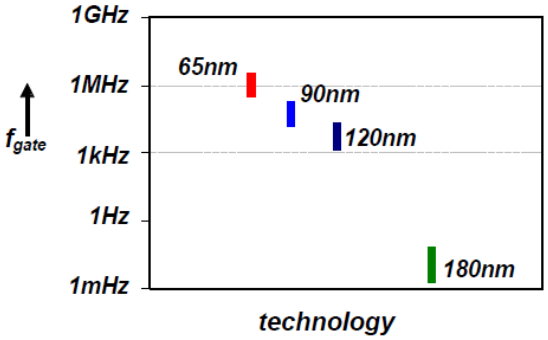


***Fig. 2:*** $f_{gate}$ *Ranges for Typical Analog Applications, for NMOS-Transistors in Different CMOS Technologies. For PMOS-Transistors* $f_{gate}$ *is roughly a Factor 3 Lower.*

Figure 2 shows $f_{gate}$-bands for four technologies as derived from measurements. This figure shows that $f_{gate}$ ranges from roughly 0.1 Hz in 180 nm technologies to about 1 MHz in 65 nm CMOS; for PMOS-transistors, $f_{gate}$ is roughly a factor 3 lower. This $f_{gate}$ can be used to easily estimate the impact of gate leakage on other relevant properties of MOS transistors.

***The Impact of Gate-Leakage on Matching***

Gate leakage is caused by quantum-mechanical tunneling and depends on the layer-thickness and the field-strength. It therefore exhibits spread that can limit the achievable level of performance of analog circuits. Because spread and mismatch are DC effects, they do not (from a fundamental point of view) require any additional power. However, the typical way to minimization is, spending area which in turn increases power consumption at a given speed[9,10], because larger capacitances have to be charged[11].

In this relation, a constant that is independent of area and (almost) independent of technology. It follows directly those high values of gate result in a large impact of gate-leakage related mismatch. The previous relation also shows that by linear scaling of transistors (increasing the width and the length proportionally), with constant power consumption, the classical mismatch term decreases while at the same time the gate-leakage term increases. This yields a maximum usable area and a lower limit on attainable mismatch. With width-scaling and a proportional power-scaling there is no minimum in the reachable mismatch figure. It's also clear that the gate has a significant impact on the minimum attainable mismatch figure: for maximum matching therefore low-leakage devices should be used.

The fully depleted transistors are basically thin-film SOI transistors that come in many flavors. Figure 4b shows the type that resembles the planar bulk device in Figure 4a the most. The double-gate variant that probably is the successor or the planar bulk devices is the FinFET[12–16] shown in Figures 4c and 4d. The naming of the FinFET originates from its appearance, (Figure 4d); the device resembles a silicon fin on top of a $SiO_2$ layer, with the gate draped over it to effectively form a gate on (usually only) both sides of the fin. Figure 3 shows the spread of an MOS transistor in 65 nm CMOS with a) linear scaling of W and L at constant power consumption b) W-scaling, and proportional power scaling.

**The Impact of Gate-Leakage on Noise**

Similarly as any current over an intersection, door spillage displays shot-commotion with current thickness. In that capacity, it is equal to base-streams in bipolar transistors. This shot noise comes on top of the induced gate noise[17,18]. Noise in the gate current therefore limits noise performance in analog circuits in UDSM CMOS[19].

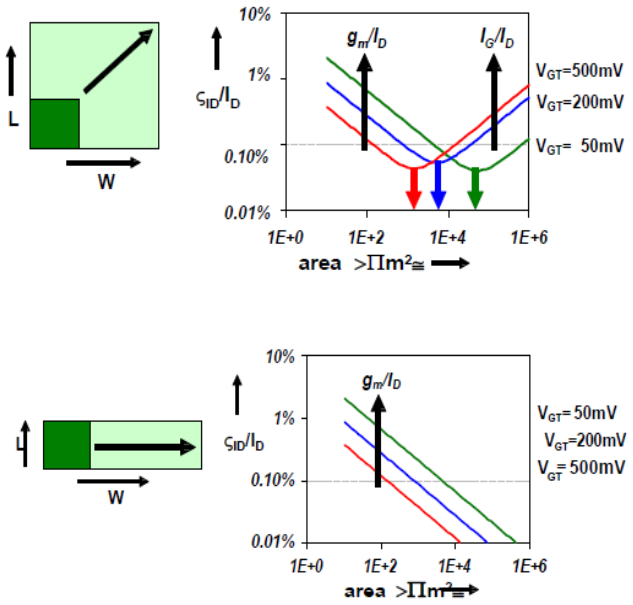


***Fig. 3:*** *The Spread of an MOS Transistor in 65 nm CMOS with* ***(a)*** *Linear Scaling of W and L at Constant Power Consumption,* ***(b)*** *W-Scaling, and Proportional Power Scaling.*

## FUTURE CMOS TRANSISTORS

In the past few decades, the transistors in mainstream CMOS technology were planar bulk devices. Scaling of these planar bulk devices is expected to end around the 45 nm technology node[20,12]. The most likely successors are fully depleted (FD) thin-body transistors[12,21].

These FD thin-body transistors have a number of advantages over conventional UDSM transistors:

a. The body of the FinFET will be almost undoped, while the threshold voltage will be determined by the work function between the silicon and the metal gate[22]. Similarly as any current over an intersection, door spillage displays shot-commotion with current thickness. In that capacity, it is equal to base-streams in bipolar transistors.
b. Vt-spread will be determined by the spread in the fin-width and by the spread in the work function [22]. There's not yet good data of expected mismatch and area-scaling relations.
c. Conduction takes place on the sidewalls of the fin, which are formed by etching this surface is rough which probably gives rise to excess flicker noise.
d. The gate-leakage of FinFETs is reduced by about one order of magnitude compared to that in planar devices because of reduced fields and quantum confinement effects[23].
e. The mobility and hence the transistor's current factor is orientation dependent in FinFETs because of the conduction on the sidewalls of the fin: the crystal orientation can be anything ranging from (1 0 0) to (1 1 0) which significantly affects carrier mobility[15,24]. This orientation dependency is expected to give no problems in analog circuit design as it is a good practice to layout matching sensitive transistors in the same orientation.
f. Heat transfer of transistors is lower in SOI transistors compared to bulk devices: the thermal conductivity of SiO2 is about two orders of magnitude lower than that of Si. For regular simple utilizations of transistors, with a moderately low door source overdrive voltage and deplete source voltage, this may bring about warming of transistors. Warming outcomes in moved transistor parameters that may bring about confuse or warm hysteresis impacts [25, 26]. For accurate analog models, the temperature may have to be included as a state-variable.

All together, the FinFETs have a number of parameters that are better than those of conventional devices: output conductance, gate-leakage and junction capacitances are lower. A number of new effects are introduced; most notably new mismatch effects, heating effects and flicker noise which introduce many unknowns in circuit design. With the current design aspects of UDSM CMOS technologies[3], this gives many new research opportunities.

## CIRCUIT DESIGN CHALLENGES AND OPPORTUNITIES

From a system point of view, analog/RF moves to either higher speeds or higher flexibility, enabling software signal processing. From a technology point of view the speed of the transistors increases, digital properties improve, while at the same time the analog properties get worse. In light of this the part of simple circuits for the future can be anticipated. In order to do so, we propose to classify four types of electronic circuits:

1. Pure digital circuits,
2. Analog circuits for computerized,
3. Digital circuits for simple,
4. Pure simple circuits.

### Pure Digital Circuits

Pure digital circuits will continue to grow in complexity. Driven by Moore's law the number of gates will grow exponentially, and cost effective ICs will exploit the high gate count. Such complex ICs are hard to oversee and this is one of the reasons why digital ICs will contain multiple cores (or tiles) of processors, memory, and dedicated digital hardware. The cores can operate in parallel [27], at locally high speeds and relatively slow networking over the "large distances". The pure digital

design work is highly automated, and higher order description languages like VHDL are common practice today. Digital designers don't have to worry much about gate level design anymore; however the challenge is to oversee such a complex system. To build up a mind boggling IC in a cutting edge innovation is extremely costly and in this way it is advantageous to utilize a similar IC (equipment) in various applications by programming its usefulness in programming. One of the immense difficulties is to program such a framework in a compelling route since parallel preparing is gravely bolstered by todays programming dialects.

Advanced approaches to expand the strength of basically computerized frameworks incorporate equality checks and ECC (blunder checking and rectifying) which are for the most part found in recollections and in correspondence channels [28].

**Analog Circuits for Digital**

Unadulterated computerized ICs contain a couple of essential genuine simple capacities like power-on-reset and a PLL for inner rapid low jitter clock era which clearly adapts to traditional simple usage issues. However likewise the "unadulterated computerized" circuits confront simple issues. One of the principal issues experienced was flag integrity[29]: advanced exchanging itself makes skip on provisions and substrate hubs in a manner that entryway speed drops altogether and even practical mistakes result. Appropriate on-chip decoupling can take care of these issues at the cost of range [29].

The power utilization of computerized ICs unequivocally relies on upon the supply voltage and the clock recurrence. To minimize control utilization, versatile supply voltages and timekeepers can be utilized. To actualize this, DC-DC converters can be utilized as a part of control frameworks where both the clock recurrence and the supply are brought down in a manner that the computation is done in the nick of time. This versatile supply can yield critical power investment funds in functional ICs [30,31].

Another utilization of rising simple control for advanced circuits is the incorporation of numerous simple circuits as sensors in expansive computerized ICs. Doing as such, resistance towards handle variety and temperature edge does not should be considered in the plan, which may spare a lot of overhead and power utilization. Examples include measuring the local supply voltage [32], the local temperature [33], jitter etc. and adapting to them. Another application of sensory electronics in combination with actuators is the cancellation of unwanted disturbances [34].

Another issue identified with power supply of advanced ICs is the similarity of new items with old ones. The inside supply voltage of ICs has been dropping the previous decade from 5 V down to 1 V today. However lingering behind, the PCB board outlines still utilize higher voltage swings and supplies as models. Consequently the cutting edge computerized ICs ought to once in a while still look, all things considered, as though they work on a higher supply voltage than utilized inside. This is particularly the case for ware items like microcontrollers. Therefore completely incorporated supply voltage controllers [35, 36] and high voltage IO buffers [37] have been created in cutting edge CMOS advancements. These circuits are outlined at a higher than ostensible supply voltage, however via painstakingly stacking gadgets the circuits can withstand the high voltages.

The on-chip correspondence is getting more consideration, as (worldwide) interconnects are quickly turning into a

speed, power and unwavering quality bottleneck for advanced frameworks [38]. Technological advances such as copper interconnects and low-k dielectrics are not sufficient to let the interconnect bandwidth keep up with the advances in transistor speeds.

From a circuit-design perspective, a general solution is the use of repeaters, which is expensive in term of area and power. Another proposed solution uses low-swing signaling over differential 10 mm aluminum interconnects [39]. Chang *et al.*, proposed to use 16 µm-wide differential wires (20 mm long) and exploit the LC regime (transmission line behavior) of these wires =[40].

Schinkel *et al.* showed that pulse-width pre-emphasis in combination with resistive termination can increase the data-rate to 3 Gb/s/ch, using 10 mm long, 0.4 µm wide differential interconnects [41]. Without the proposed techniques, these interconnects can achieve only 0.55 Gb/s/ch. So by using analog equalizers which still comply with pure digital swing, a factor 6 in speed increase can be achieved over large distances.

**Digital Circuits for Analog**

Analog CMOS circuits typically reside on an IC that has digital signal processing circuits. Since digital circuits have become very compact, analog circuits can nowadays receive help from digital circuits: the analog circuits can be calibrated and can be corrected for the non-ideal behavior. This calibration can be online, while normal signals are processed, or offline in a special calibration mode. This correction in turn can be done in the analog domain (where typically a DA converter injects a static signal in the analog circuit) or in the digital domain (where an error can be subtracted). Below some examples of calibrated circuits are given. This trend of calibrating is clearly observable in AD converters. This allows the use of simple power efficient open-loop residue amplifiers, which are more compatible with modern CMOS technologies. ADCs can even be calibrated on line in background, with a calibrated auxiliary ADC. Wang *et al*. showed, a pipelined analog-to-digital converter (ADC) is calibrated in background using an algorithmic ADC, which is it calibrated in foreground[42]. The calibration overcomes the circuit non-idealities caused by capacitor mismatch and finite operational amplifier (opamp) gain both in the pipelined ADC and the algorithmic ADC. Digital calibration is also used in RF circuits: for example Brenna *et al.* presented calibrations techniques that suppress the carrier leakage and enable the direct-up conversion architecture to meet WCDMA specifications [43].

Another example is given by Mehta *et al.*, where a closed-loop RF calibration is used in a fully integrated transceiver, including digital MAC layers [6]. An RF loop-back path is used from the output of the transmit mixer to the input of the receive mixer. During calibration, a known digital sequence is transmitted and looped back to the receiver and the received digital signal is used to correct for analog and RF non-idealities such as DC offset, I/Q mismatch, and RF carrier leak. This way matching requirements are relaxed and area and power can be saved.

If we observe this trend, then we can foresee analog circuits, with many calibration points. Smart algorithms can locate the error sources in the digital domain and correct for it. This way, at least static errors (gain, mismatch, and even linearity) can be compensated. However, noise cannot be compensated for in the digital domain due to its wide band nature: it remains an analog problem. On the system level, however, detection algorithms can be improved so that less signal-to-noise is needed for the required bit error rate. For example in RF circuits,

inductors are used today to improve the signal to noise ratio. If we realize that an inductor of a few nH; which is necessary for the low GHz range occupies the same die area as a simple baseband processor in 65 nm technology, it is clear that smart digital detection techniques can help to overcome noise problems as well.

**Pure Analog Circuits**

Analog once was the field in which the main chunk of signal processing was done. Since a couple of decades a nonstop move towards advanced flag preparing with some simple handling (or molding) of the information sources and yields of the computerized center is clear. Be that as it may, even now simple circuits are required to get important information into and out of the advanced center in a territory productive and control effective way. Despite the fact that the range where unadulterated simple is connected will unavoidably psychologist to a (non-zero) least, the prerequisites on simple circuits will keep on increasing while the CMOS usage environment deteriorates and more awful.

One fundamental problem for analog CMOS circuits is the lowering supply voltage. This problem can be tackled in two ways. Outline simple circuits that work at a low voltage or plan simple circuits that can withstand higher than ostensible supply voltages.

The primary approach was well known amid the previous 15 years where the supply dropped from 5 V down to 1.2 V today. Numerous new circuit procedures have been created as of late, for instance the exchanged opamp method where switches in exchanged capacitor are moved from the flag way to the supply way, where they require less door drive [44]. Recently a similar approach has been demonstrated for Gilbert type of mixers [45].

Despite all the research effort, today the bare minimum supply for an analog circuit seems to be VGS+VDSSAT+*v* swing, where *v* swing is the signal swing. If still enough SNR is needed then the noise has to be lowered. This can simply be done via impedance level scaling, and the result is that 10 dB less noise will result in 10 times more power consumption (for the same supply voltage, SINAD, bandwidth, etc.).

Thermal noise can even be cancelled but also at the cost of power dissipation[46]. 1/f noise is a major concern as well since the corner frequency, where thermal noise dominates the 1/f noise seems to be proportional to ft. in a given technology. So since ft is usually chosen high, to benefit from the bandwidth, 1/f noise will be large as well. Chopping and double correlated sampling can remove 1/f noise for low frequency application. Switched bias technique can reduce the intrinsic 1/f noise of transistors [47].

The second approach is to configuration circuits that can withstand higher than ostensible supply voltages. This is typically done through stacking of transistors while taking consideration that every transistor does not breakdown, including amid homeless people and startup.

These circuits at higher supply were first found in interfacing drivers[37] and later in (RF) PAs[48,49], but nowadays also normal "internal" analog circuits need to use these techniques to get performance at today's 1 V supply voltage. This can be done, but careful simulation has to be done by the designers, because moderate breakdown effects are hard to see during production test and may show up during the lifetime of the IC.

Analog circuits will operate at higher frequencies as well. At high frequencies it's beneficial to use inductors for high Q circuits, like oscillators and tuned

amplifiers Inductor quality factors (Q) increase with frequency and at frequencies beyond say 40 GHz Q factors of integrated spiral inductors are higher than the Q factors of the resonating capacitors. Realizing this, the designer does not have to take care for max Q of inductors, and also since that the values of inductances are small for high frequencies, the inductors can be laid out in a very compact way: for example in a compact U shape instead of a circle[50–54]. So for very high frequencies inductors can be used at many nodes in a circuit.

**Wrap Up**

In the past decades, much functionality shifted from the (traditional) analog domain to the digital domain because of (area and power) efficiency reasons. Apart from this shift, there is also a clear trend towards mixing analog and digital. In the near future high-performance digital blocks include analog sensory and control systems, while analog circuits tend to include more and more digital compensation and control.

***Table 1:*** *Control and Function of ICs*

| | | **Controlled:** | |
|---|---|---|---|
| | | **Analog** | **Digital** |
| **Function:** | **Digital** | Adaptive clock adaptive supply voltage measure temperature measure local various decrease local noise multi-level I/O on-chip modems. | Redundancy parity bit ECC. |
| | **Analogue** | Chopping switched circuits switched bias noise cancelling “high-voltage” circuit analog calibration DEM. | Digital calibration pre-distortion post Processing. |

## CONCLUSIONS

The development of CMOS innovation will proceed for a long time to come, which is advantageous for advanced circuits yet which is not so for simple. A broad talk of generally new non-perfect impacts, for example, door spillage and yield conductance is given in this paper, similar to an examination of the most likely successor of the routine MOS transistor.

On the basis of system level, there have been trends for shifting functionalities from analog to digital domains. And the trend would continue and the domains will go off. The importance of circuit performance will be more which will yield a clear trend of each domain for analog and digital control and vice versa.

## REFERENCES


1. Taur Y. CMOS Design Near the Limit of Scaling. *IBM J. Res. & Dev.* 2002; 46(2/3): 213–222p.
2. Buss DD. Technology in the Internet Age. In *Dig. Tech. Papers, ISSCC.* 2002; 18–21p.
3. Annema AJ, Nauta B, van Langevelde R, *et al.* Designing Outside Rails Constraints. In *Dig. Tech. Papers, ISSCC*. 2004; 134–135p.
4. van Zeijl P, Eikenbroek JWTh, Vervoort PP, *et al.* A Bluetooth Radio in 0.18-µm CMOS. *IEEE J. Solid-State Circuits*. Dec 2002; 37: 1679–1687p.
5. Darabi H, Khorram S, Zhou Z, *et al.* A Fully Integrated SoC for 802.11 b in 0.18 um CMOS. In *Dig. Tech. Papers, ISSCC.* 2005; 96–97p.
6. Mehta S, Weber D, Terrovitis M, *et al.* 802.11 g WLAN SoC. In *Dig. Tech. Papers, ISSCC.* 2005; 94–95p.

7. Adiseno, Ismail M, Olsson H. A Wide-Band RF Front-End for Multiband Multistandard High-Linearity Low-IF Wireless Receivers. *IEEE J. Solid-State Circuits*. Sep 2002; 37: 1162–1168p.
8. Arkesteijn VJ, Klumperink EAM, Nauta B. A Wideband High-Linearity RF Receiver Front-End in CMOS. In *Proc. ESSCIRC*. 2004; 71–74p.
9. Pelgrom MJM, Tuinhout HP, Vertregt M. Transistor Matching in Analog CMOS Applications. In *IEDM Tech Dig*. 1998; 915–918p.
10. Pelgrom MJM, Duinmaijer ACJ, Welbers APG. Matching Properties of MOS Transistors. *IEEE J. Solid-State Circuits*. 1989; 24(10): 1433–1440p.
11. Bult K. Analog Design in Deep Sub-Micron CMOS. In *Proc. ESSCIRC*. 2000; 11–17p.
12. Skotnicki T, Hutchby JA, King TJ, *et al.* The End of CMOS Scaling. *IEEE Circuits Devices Mag*. Jan 2005; 16–26p.
13. Hisamoto D, Kaga T, Kawamoto Y, *et al.* A Fully Depleted Lean-channel Transistor (DELTA)-A Novel Vertical Ultra Thin SOI MOSFET. In *Proc. IEDM*. 1989; 833–836p.
14. Hisamoto D, Lee WC, Kedzierski J, *et al.* FinFET-A Self-Aligned Double-Gate MOSFET Scalable Beyond 20 nm. *IEEE Trans. Electron Dev*. Dec 2000; 2320–2325p.
15. Nowak EJ, Aller I, Ludwig T, *et al.* Turning Silicon on its Edge. *IEEE Circuits Devices Mag*. Jan 2004; 20–31p.
16. Huang X, Lee WC, Kuo C, *et al.* Sub-50 nm P-Channel FinFET. *IEEE Trans. Electron Dev*. May 2001; 48: 880–886p.
17. Scholten AJ, Tiemeijer LF, van Langevelde R, *et al.* Noise Modeling for RF CMOS Circuit Simulation. *IEEE Trans. Electron Dev*. 2003; ED-50(3): 618–632p.
18. van Langevelde R, Paasschens JCJ, Scholten AJ, *et al.* New Compact Model for Induced Gate Current Noise. In *IEDM Tech Dig*. 2003; 867–870p.
19. Stek A, de Jong GW, Jansen TPHG, *et al.* Circuit Design and Noise Considerations for Future Blu-ray Disc Optical Storage Technology. In *Dig. Tech. Papers, ISSCC*. 2004; 136–137p.
20. Boeuf F, Arnaud F, Basso MT, *et al.* A Conventional 45 nm CMOS Node Low-Cost Platform for General Purpose and Low Power Application. In *Proc. IEDM 2004*. Dec 2004; 425–428p.
21. Chang L, Choi YK, Kedzierski J, *et al.* Moore's Law Lives on. *IEEE Circuits Devices Mag*. Jan 2003; 35–42p.
22. Xiong S, Bokor J. Sensitivity of Double-Gate and FinFET Devices to Process Variations. *IEEE Trans. Electron Dev*. Nov 2003; 2255–2261p.
23. Chang L, Yang KJ, Yeo YC, *et al.* Direct-Tunneling Gate Leakage Current in Double-Gate and Ultrathin Body MOSFETs. *IEEE Trans. Electron Dev.* Dec 2002; 12: 2288–2294p.
24. Chang L, Ieong M, Yang M. CMOS Circuit Performance Enhancement by Surface Orientation Optimization. *IEEE Trans. Electron Dev.* Oct 2004; 51: 1621–1627p.
25. Pop E, Dutton R, Goodson K. Thermal Analysis of Ultra-Thin Body Device Scaling. In *Proc IEDM*. 2003; 883–886p.
26. Tenbroek BM, Redman-White W, Lee MSL, *et al.* Characterization of Layout Dependent Thermal Coupling in SOI CMOS Current Mirrors. *IEEE Trans. Electron Dev*. Dec 1996; 43(12): 2227–2232p.
27. Horowitz M, Dally W. How Scaling will Change Processor Architecture. In *Dig. Tech. Papers ISSCC*. 2004; 132–133p.
28. Agarwal A, Paul BC, Roy K. Process Variation in Nano-Scale Memories: Failure Analysis and Process Tolerant

Architecture. In *Proc. CICC*. 2004; 353–356p.
29. Veendrick H. Digital Goes Analog. In *Proc. ESSCIRC*. 1998; 44–50p.
30. Kim J, Horowitz MA. An Efficient Digital Sliding Controller for Adaptive Power-Supply Regulation. *IEEE J. Solid-State Circuits*. May 2002; 37: 639–647p.
31. Nakai M, Akui S, Seno K, *et al.* Dynamic Voltage and Frequency Management for a Low-Power Embedded Microprocessor. *IEEE J. Solid-State Circuits*. Jan 2005; 40: 28–35p.
32. Muhtaroglu A, Taylor G, Rahal-Arabi T. On-Die Froop Detector for Analog Sensing of Power Supply Noise. *IEEE J. Solid-State Circuits*. Apr 2004; 4: 651–660p.
33. Schinkel D, de Boer RP, Annema AJ, *et al.* A 1-V 15µW High-Precision Temperature Switch. In *Proc. ESSCIRC*. 2001; 104–107p.
34. Tsukada T, Hashimoto Y, Sakata K, *et al.* An On-Chip Active Decoupling Circuit to Suppress Crosstalk in Deep-Submicron CMOS Mixed-Signal SoCs. *IEEE J. Solid-State Circuits*. Jan 2005; 40: 67–79p.
35. den Besten GW, Nauta B. Embedded 5 V-to-3.3 V Voltage Regulator for Supplying Digital IC's in 3.3 V CMOS Technology. *IEEE J. Solid-State Circuits*. Jul 1998; 33: 956–962p.
36. Hazucha P, Karnik T, Bloechel B, *et al.* An Area-Efficient, Integrated, Linear Regulator with Ultra-Fast Load Regulation. *Symp. VLSI Circuits Dig.* Jun 2004; 18: 218–221p.
37. Annema AJ, Geelen GJGM, de Jong PC. 5.5 V I/O in a 2.5-V 0.25-µm CMOS Technology. *IEEE J. Solid-State Circuits*. Mar 2001; 36: 528–538p.
38. Ho R, Mai KW, Horowitz M. The Future of Wires. *Proc. IEEE*. Apr 2001; 490–504p.
39. Ho R, Mai K, Horowitz M. Efficient On-Chip Global Interconnects. *2003 VLSI Circuits Symposium*. Jun 2003; 271–274p.
40. Chang RT, Talwalkar N, Yue CP, *et al.* Near Speed-of-Light Signaling Over On-Chip Electrical Interconnects. *IEEE J. Solid-State Circuits.* May, 2003; 38: 834–838p.
41. Schinkel D, Mensink E, Klumperink EAM, *et al.* A 3Gb/s/ch Trnasceiver for RC-Limited On-Chip Interconnects. *ISSCC.* 2005; 386–387p.
42. Wang X, Hurst PJ, Lewis SH. A 12-Bit 20-M Sample/s Pipelined Analog-to-Digital Converter with Nested Digital Background Calibration. *IEEE J. Solid-State Circuits*. Nov 2004; 39: 1799–1808p.
43. Brenna G, Tschopp D, Rogin J, *et al.* A 2-GHz Carrier Leakage Calibrated Direct-Conversion WCDMA Transmitter in 0.13-µm CMOS. *IEEE J. Solid-State Circuits*. Aug 2004; 39: 1253–1262p.
44. Crols J, Steyaert M. Switched-Opamp: An Approach to Realize Full CMOS Switched-Capacitor Circuits at Very Low Power Supply Voltages. *IEEE J. Solid-State Circuits*. Aug 1994; 29: 936–942p.
45. Klumperink EAM, Louwsma SM, Wienk GJM, *et al.* A CMOS Switched Transconductor Mixer. *IEEE J. Solid-State Circuits*. Aug 2004; 39: 1231–1240p.
46. Bruccoleri F, Klumperink EAM, Nauta B. Wide-Band CMOS Low-Noise Amplifier Exploiting Thermal Noise Canceling. *IEEE J. Solid-State Circuits*. Feb 2004; 39: 275–282p.
47. van der Wel AP, Klumperink EAM, Vandamme LKJ, *et al.* Modeling Random Telegraph Noise Under Switched Bias Conditions Using Cyclostationary RTS Noise. *IEEE Trans. Electron Dev*. May 2003; 50: 1378–1384p.
48. Sowlati T, Leenarts DMW. A 2.4-GHz 0.18-um CMOS Self-Biased Cascode Power Amplifier. *IEEE J.*

*Solid-State Circuits*. Aug 2003; 38: 1318–1324p.

49. Serneels B, Piessens T, Steyaert M, *et al. A High Voltage Output Driver in a 2.5 V 0.25 um CMOS Technology*. 2005: 576–583p.
50. van der Wel AP, Gierkink SLJ, Frye RC, *et al.* A Robust 43-GHz VCO in CMOS for OC-768 SONET Applications. *IEEE J. Solid-State Circuits*. Jul 2004; 39: 1159–1163p.
51. Dubois J, Knol J, Bolt M, *et al.* Impact of Source/Drain Implants on Threshold Voltage Matching in Deep Sub-Micron CMOS Technologies. In *Proc. ESSDERC*. 2002; 115–118p.
52. Nowak EJ. Maintaining the Benefits of CMOS Scaling When Scaling Bogs Down. *IBM J. Res. & Dev.* Mar 2002; 46: 169–179p.
53. Ananthan H, Bansal A, Roy K. FinFET SRAM Device and Circuit Design Considerations. In *Proc. 5th Int'l Symposium on Quality Electronic Design*. 2004; 511–516p.
54. Murmann B, Boser BE. A 12-Bit 75-MS/s Pipelined ADC Using Open-Loop Residue Amplification. *IEEE J. Solid-State Circuits.* Dec 2003; 38: 2040–2050p.